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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,552	02/27/2002	Hiroshi Nakamura	001701.00672	8483

22907 7590 03/25/2003

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/083,552	NAKAMURA, HIROSHI	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/656831* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/05/2003 has been entered. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bill et al. (USP 5059815).

As to claims 1, 11, 21 and 22, Bill et al. discloses in figure 3 a circuit comprising: a boost unit group including a plurality of boost units (350, 360) series-connected between input node (C) and node VOUT; a first transistor (310) connected between the input node and a node for receiving a first voltage (Vpp), wherein each boost unit has input and output portions, a second transistor having a both gate and a drain connected to the input portion and a source connected to the output portion, and a second capacitor (C3, C4) in each boost unit connected to the input portion, a source of the second transistor of the first boost unit being directly connected to the

input portion of the second boost unit, and a gate of the first transistor is directly connected to the input portion of one of boost unit (360). Thus, figure 3 shows all limitations of the claims except for a first capacitor having one end which is connected to an output node, and another end which is receives a first oscillation signal. However, Bill et al.'s abstract teaches that a number charge pump circuits may be cascaded to form a multi-stage charge pump circuit. Therefore, it would have been obvious to one having ordinary skill in the art to cascade plurality of charge pump circuits figure 3 for the purpose of forming a multi-stage charge pump circuit. Thus, node D in the second charge pump circuit, which cascaded to the first charge pump circuit figure 3, is the output node, and capacitor C4 of the second stage having one end which is connected to the output node, and another end which receives a first oscillation signal (/Φ).

As to claims 2 and 12, Bill et al.'s figures 1a and 3 show all limitations of the claim except for the boost unit group includes not less than three boost units. However, it is notorious well known in the art the output voltage of the charge pump circuit is determined by the number of boost units. Therefore, the selection for the boost unit to have not less than three boost units is seen as a matter of design choice depending on the design output level voltage (column 3, lines 15-25 also teaches number of boosting unit is a matter of design choice).

As to claims 3, 10, 13 and 20, figure 2 shows a third transistor (250) which has a gate connected to the output node, and transfers a third voltage (VppI), wherein a second voltage at the gate of the third transistor is equal to, or larger than a sum of the third voltage and a threshold voltage of the third transistor (V270 = VppI + Vgate-source, wherein Vgate-source = threshold voltage) in transferring the third voltage.

As to claims 4 and 14, figure 3 shows a second oscillation signal /Φ is input to an even-numbered boost unit from the input node, a third oscillation signal ϕ is input to an odd-numbered boost unit from the input node, and the second and third oscillation signals have opposite phases or different timings.

As to claims 5 and 15, it is inherent for gate and source voltage levels of the first transistor gradually rise while changing in opposite phases.

As to claims 6 and 16, figure 3 shows a circuit (340) for fixing the gate of the first transistor to low level in an OFF state.

As to claims 7-9 and 17-19, figures 1a and 3 show all limitations of the claims except for a threshold voltage of the second transistor in at least one of the boost units is lower than a threshold voltage of the first transistor; or a transistor having a threshold voltage lower than the threshold voltage of the first transistor is arranged in a boost unit closest to the output node; a threshold voltage of a transistor in a boost unit on the output node side is lower than a threshold voltage of a transistor in a boost unit on the input node side. However, it is well known in the art that threshold of the diode connected transistors e.g. 350, 360... determined the level of the voltage output. Therefore, it would have been obvious to one having skill in the art to select the threshold of all diode connected transistors in the boost unit to be less than the threshold of the first transistor for the purpose of reducing the output voltage level.

As to claims 23 and 24, figure 3 shows the first oscillation signal and an oscillation signal (Φ) which is input to the boost unit connected to the first capacitor have opposite phased or different timings.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
March 19, 2003

Terry D. Cunningham
Primary Examiner